## Plasma Texturing of Multiple Kerf-Less Separated Ultra-Thin Silicon Layers Alena Okhorzina<sup>1</sup>, Richard Schalinski<sup>1,2</sup>, Norbert Bernhard<sup>1</sup>, Stefan L. Schweizer<sup>2</sup>

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**Abstract:** Kerf-less separated ultra-thin silicon layers are an interesting future perspective for ultra-thin silicon solar cells, but difficult to texture by the classical wet-chemical processes, because the initial micro-roughness of the surface due to the sawing process is missing. In this investigation it is demonstrated that multiple kerf-less separated ultra-thin silicon layers can be textured by a mask-less plasma etching process. The silicon layers were separated by the so-called millefeuille process in which modulated photo-electrochemically etched macro-pores grow in a subsequent tempering process which leads to separation of several ultra-thin silicon layers.

**Aim and approach:** It was the aim to investigate whether plasma etching would be a suited method to texture ultra-thin silicon layers such effectively that they could be used for photovoltaic applications. For this purpose the millefeuille process of Hernandez and co-workers [1] was adopted. This process is based on photo-electrochemical etching (PECE) [2], but uses a modulation of voltage and photocurrent to create periodically wide and narrow pores. In a subsequent anneal step under hydrogen or inert gas atmosphere the pores re-arrange by Si diffusion. Under appropriate conditions the wide pores grow together and several thin silicon layers are separated. These thin layers with rather smooth surface are then transferred to a plasma etch system and textured by a mask-less plasma etch process (so-called black-silicon process [3]).

**Results and conclusions:** With a combined capacitive and inductive coupling of the high-frequency (13.56 MHz) generator to the plasma an aspect ratio of more than one with typical sizes in the range of 100 to 200 nm could be reached, a texturing which is known to act as a very effective light trapping structure, as studied previously on thicker layers [3, 4]. In order to generate the multiple thin layers with typical thicknesses in the range of 10 to 20 µm several process optimization steps, especially of the tempering step were necessary. A separation of up to four layers at the same time was reached, although the separation and layer quality was not yet perfect across larger areas. Main problems were remaining pores in some layers and also thin connection bridges below neighbouring layers. But all the same, the principal feasibility of the process was shown.

## **Explanatory pages:**

The current industrial main stream process of the separation of ingots to slices (wafering) for crystalline silicon solar cells is diamond-wire sawing. This process causes a micro-rough and damaged surface, which afterwards is usually wet-chemically etched in order to remove the saw damage and create effective light-trapping structures for reflectivity reduction and increasing the effective mean path length of the incident light. Since the relative material loss of sawing increases with decreasing wafer thicknesses, and also the process itself is limited, if wafer thicknesses become too low due to mechanical stability reasons, an increasing several attempts in investigating so-called kerf-less separation techniques (i.e. without loss of Si material) were made. Besides hydrogen implantation (SmartCut [5]), deposition of a ductile metal (SlimCut [6]), the photo-electrochemical growth of pores (PorousCut [7, 8]) is a promising technique. By Hernandez and co-workers it was shown that the PorousCut technique could be run in such a way that several layers could by separated at the same time [1], a process which could improve the productivity in case of a possible future volume production (fig. 1). Since the layered structure resembles puff pastry (in French millefeuille) the authors called it millefeuille process.



Figure 1: Schematic flow of the millefeuille process. After creating the modulated porous structure, an anneal step leads to re-arrangement of Si atoms and finally to complete separation of several layers.

Fig. 2 shows the separation of several layers as it was reached within this investigation after several optimization steps of the anneal, the process parameter of which turned out to be very critical for a good separation and good layer quality. As also visible in fig. 2, the surfaces of the layers are rather smooth, which means that a wet-chemical process which needs an initial roughness as points of etch attack would not work well. But it is known that plasma etching works almost independent of crystallographic orientation and also for perfectly smooth wafers [3, 4]. Therefore plasma etch processes which were already widely investigated

on wafers of normal thickness with promising performance [3, 4] were applied to the thin millefeuille layers. For this purpose a special sample holder was designed, by which a millefeuille layer could be transferred on a plasma resistant tape to the plasma etch chamber. This chamber had the possibility of superimposing a capacitively coupled plasma (CCP) and an inductively coupled plasma (ICP) at the same time. Whereas in pure CCP the self-bias (determining the ion energy of bombarding ions) and the plasma density (determining the amount of ions and chemically etching radicals) are inherently connected to each other, by applying a superposition of CCP and ICP both parameters can be independently changed, opening a greater window of possible process results and especially aspect ratios of the texturing. A high CCP contribution gives very high aspect ratios (almost needle like structures), a fair balance between CCP and ICP gives moderate aspect ratios (similar to wet chemical etching) [3, 4].



Figure 2: SEM picture of a multiple layer generated by the millefeuille process. A good layer separation and a good lateral homogeneity is visible.

Fig. 3 show the SEM cross section of a plasma textured wafer with SF6/O2 chemistry and CCP and ICP excitation superimposed. A texturing with moderate aspect ratio was chosen, because this is a good compromise between reflectivity reduction and a reasonable charge carrier lifetime after surface passivation [4].



Figure 3: SEM cross section of the plasma textured surface. Clearly visible the reflection reducing surface topography with structures in the range 100 to 150 nm width and roughly 200 nm height.

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